UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,587	07/22/2003	Scott Dickson	990467	7742

23696 7590 03/20/2007
QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
SOBUTKA, PHILIP	
ART UNIT	PAPER NUMBER
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/20/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/20/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

us-docketing@qualcomm.com
kascanla@qualcomm.com
t_ssadik@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	10/625,587	DICKSON, SCOTT	
	Examiner	Art Unit	
	Philip J. Sobutka	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,12-16,25-27 and 36-38* is/are rejected.

7)☒ Claim(s) *4-11,17-24 and 28-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1,12,13,36 are rejected under 35 U.S.C. 102(e) as being anticipated by Baker et al (US 6,556,838).

Consider claim 1. Baker teaches a method comprising:

keeping a running history, up to a predetermined length, of power control instructions included in a first plurality frames received in one direction on a link of a channel, the first frames being queued before processing *(Baker see column 2, lines 46-67, note that Baker teaches combining power control slots, or frames see especially column 4, lines 30-67)*; and

generating power control commands for a second plurality of frames to be transmitted on a return direction of the channel, based at least in part on the running history being kept, in a manner that effectuates a slowing of response to the incoming power control instructions, the second frames also being batched for subsequent processing in batch form for transmission *(note that the adjusted step size of Baker*

would result in a slowing of response under the appropriate conditions see figure 2, column 4, lines 38-67, column 5, lines 35 – column 6, line 65).

Note the Baker teaches the power control equals two bits *(Baker see column 3, line 63).* Note that a two bit command would comprise m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second frames, with m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", m and n being integers.

As to claim 12, note that Baker teaches the operations being performed in a gateway of a wireless communication system *(Baker teaches that one station could be a base station, or gateway, see column 1, lines 65 – column 2, line 11).*

As to claim 13, note that Baker teaches the operations are being performed in an emulated gateway and a gateway simulator of a wireless communication test system *(Note that Baker's arrangement is an emulator see column 2, lines 47-57).*

Consider claim 36. Baker teaches an apparatus comprising: means for keeping a running history, up to a predetermined length, of power control instructions included in a first plurality frames received on a first link of a channel, the first frames being grouped before their processing *(Baker see column 2, lines 46-67, note that Baker teaches combining power control slots, or frames see especially column 4, lines 30-67)*; and means for generating power control commands for a second plurality of frames to be transmitted on a second link of the channel, based at least in part on the running history

being kept, in a manner that effectuate slowing response to the incoming power control instructions, the second frames also being grouped for subsequent processing in batch for transmission *(note that the adjusted step size of Baker would result in a slowing of response under the appropriate conditions see figure 2, column 4, lines 38-67, column 5, lines 35 – column 6, line 65)*. Note the Baker teaches the power control equals two bits *(Baker see column 3, line 63)*. Note that a two bit command would comprise m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second frames, with m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", m and n being integers.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 14-16,25-27,37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al (US 6,556,838).

As to claim 14, Baker teaches a gateway of a wireless communication system *(Baker teaches that one station could be a base station, or gateway, see column 1, lines 65 – column 2, line 11)* comprising:

a first plurality frames on a first link of a channel, and each of said first frames include a power control instruction, and the transceiver outputting the power control

instruction included in each of said first frames *(Baker see column 2, lines 46-67, note that Baker teaches combining power control slots, or frames see especially column 4, lines 30-67)*;

generating a second plurality of frames for a second link of the channel, wherein the system keeps a running history, up to a predetermined length, of the power control instructions included in the first frames, and generate power control commands for the second frames based at least in part on the running history being kept, in a manner that effectuates slowing of responding to the incoming power control instructions *(note that the adjusted step size of Baker would result in a slowing of response under the appropriate conditions see figure 2, column 4, lines 38-67, column 5, lines 35 – column 6, line 65)*.

Baker lacks a teaching of the gateway including a batch transceiver and processor for performing the process and batching the frames for transmission. Official Notice is taken that it is notoriously well known in the art to use batch transceivers and processor to perform communication processing. Therefore it would have been obvious to one of ordinary skill in the art to modify Baker as shown in the claims in order to utilize conventional circuitry arrangement to perform the process.

As to claim 15, note the Baker teaches the power control equals two bits *(Baker see column 3, line 63)*.

As to claim 16, note the Baker teaches the power control equals two bits *(Baker see column 3, line 63)*. Note that a two bit command would comprise m "zero" value power control bits and n "one" value power control bits for each batch formed with a

subset of the second frames, with m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", m and n being integers.

As to claim 25, Baker teaches a wireless communication system, comprising:

a gateway *(Baker teaches that one station could be a base station, or gateway, see column 1, lines 65 – column 2, line 11)* receiving a first plurality frames in one direction on a link of a channel, and queuing the first frames, each of said first frames including a power control instruction *(Baker see column 2, lines 46-67, note that Baker teaches combining power control slots, or frames see especially column 4, lines 30-67)*, and

the gateway generating a second plurality of frames for transfer in an opposite direction on a link of the channel, wherein the gateway: maintains a running history over a predetermined length, of the power control instructions included with the first frames, and generates power control commands for the second frames based at least in part on the running history being kept, in a manner that effectuates a slowing of response to the incoming power control instructions *(note that the adjusted step size of Baker would result in a slowing of response under the appropriate conditions see figure 2, column 4, lines 38-67, column 5, lines 35 – column 6, line 65)*.

Baker lacks a teaching of the arrangement being a testing system performed by emulators and simulators. Official Notice is taken that it is notoriously well known in the art to use emulation and simulation to test communication system arrangements. Therefore it would have been obvious to one of ordinary skill in the art to modify Baker

as shown in the claims in order to test the communication system before it was actually implemented.

As to claim 26, note the Baker teaches the power control equals two bits *(Baker see column 3, line 63)*.

As to claim 27, note the Baker teaches the power control equals two bits *(Baker see column 3, line 63)*. Note that a two bit command would comprise m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second frames, with m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", m and n being integers.

Consider claim 37. Baker teaches a method comprising: keeping a running history, up to a predetermined length, of power control instructions included in a first plurality frames received on a first link of a channel, the first frames being grouped before their processing *(Baker see column 2, lines 46-67, note that Baker teaches combining power control slots, or frames see especially column 4, lines 30-67)*; and generating power control commands for a second plurality of frames to be transmitted on a second link of the channel, based at least in part on the running history being kept, in a manner that effectuate slowing response to the incoming power control instructions, the second frames also being grouped for subsequent processing in batch for transmission *(note that the adjusted step size of Baker would result in a slowing of response under the appropriate conditions see figure 2, column 4, lines 38-67, column 5, lines 35 – column 6, line 65)*. Note the Baker teaches the power control equals two

bits *(Baker see column 3, line 63)*. Note that a two bit command would comprise m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second frames, with m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", m and n being integers.

Baker lacks a teaching of the method being stored on machine-readable media as executable instructions. Official Notice is taken that it is notoriously well know in the art to store methods as executable instructions on machine-readable media. Therefore it would have been obvious to one of ordinary skill in the art to modify Baker to store the method as instruction on machine-readable media in order to allow the method to be easily transferred to a new machine.

Consider claim 38. Baker teaches a method comprising: emulating a gateway including receipt of a first plurality frames on a first link of a channel, and grouping said first frames for processing in batch form, each of said first frames including a power control instruction, and outputting the power control instruction includes in each of said first frames *(Baker see column 2, lines 46-67, note that Baker teaches combining power control slots, or frames see especially column 4, lines 30-67)*; a gateway simulator coupled to the gateway emulator *(Baker teaches that one station could be a base station, or gateway, see column 1, lines 65 – column 2, line 11. Note that Baker's arrangement is an emulator see column 2, lines 47-57)* to process the batched first frames in batch and to receive the power control instructions of the first frames outputted by the gateway emulator, and to generate a second plurality of frames for a

second link of the channel, the second plurality of frames also being batched before being handled by the gateway emulator in batch, wherein the gateway simulator keeps a running history, up to a predetermined length, of the power control instructions included in the first frames, and generate power control commands for the second frames based at least in part on the running history being kept, in a manner that effectuates slowing of responding to the incoming power control instructions *(Baker see column 2, lines 46-67, note that Baker teaches combining power control slots, or frames see especially column 4, lines 30-67)*. Note the Baker teaches the power control equals two bits *(Baker see column 3, line 63)*. Note that a two bit command would comprise m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second frames, with m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10", m and n being integers.

Baker lacks a teaching of the method being stored on machine-readable media as executable instructions. Official Notice is taken that it is notoriously well know in the art to store methods as executable instructions on machine-readable media. Therefore it would have been obvious to one of ordinary skill in the art to modify Baker to store the method as instruction on machine-readable media in order to allow the method to be easily transferred to a new machine.

Allowable Subject Matter

5. Claims 4-11,17-24,28-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Consider claim 4, the nearest prior art as shown in Baker fails to teach the method of claim 3, wherein if each batch of the subset of the second frames contains an even number of frames, m and n are equal.

Consider claim 5, the nearest prior art as shown in Baker fails to teach the method of claim 3, wherein if each batch of the subset of the second frames contains an odd number of frames, m and n differ by 1.

Consider claim 8, the nearest prior art as shown in Baker fails to teach the method of claim 1, wherein said generating comprises alternating between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11".

Consider claim 10, the nearest prior art as shown in Baker fails to teach the method of claim 1, wherein said generating comprises alternating between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00".

Consider claim 17, the nearest prior art as shown in Baker fails to teach the gateway of claim 16, wherein the processing subsystem is designed to generate equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames.

Consider claim 18, the nearest prior art as shown in Baker fails to teach the gateway of claim 16, wherein the processing subsystem is designed to generate a selected one of one more "zero" value power control bit and one more "one" value power control bit, if each batch of the subset of the second frames contains an odd number of frames.

Consider claim 21, the nearest prior art as shown in Baker fails to teach the gateway of claim 15, wherein the processing subsystem is designed to alternate between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11".

Consider claim 23, the nearest prior art as shown in Baker fails to teach the gateway of claim 15, wherein the processing subsystem is designed to alternate between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00".

Consider claim 28, the nearest prior art as shown in Baker fails to teach the wireless communication testing system of claim 27, wherein the gateway simulator is designed to generate equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames.

Consider claim 29, the nearest prior art as shown in Baker fails to teach the wireless communication testing system of claim 27, wherein the gateway simulator is designed to generate a selected one of one more "zero" value power control bit and one more "one" value power control bit, if each batch of the subset of the second frames contains an odd number of frames.

Consider claim 32, the nearest prior art as shown in Baker fails to teach the wireless communication testing system of claim 26, wherein the gateway simulator is designed to alternate between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11".

Consider claim 34, the nearest prior art as shown in Baker fails to teach the wireless communication testing system of claim 26, wherein the gateway simulator is designed to alternate between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00".

Response to Amendment

6. Applicant's arguments with respect to claims 1,12-16,12-16,25-27,36-38 have been considered but are moot in view of the new ground(s) of rejection.

7. Note that upon further consideration, the claims were not felt to distinguish over the cited art, therefore the allowability of certain claims has been withdrawn, and this action is not being made final.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip J Sobutka whose telephone number is 571-272-7887. The examiner can normally be reached Monday through Friday from 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew D. Anderson can be reached on 571-272-4711.

9. The central fax phone number for the Office is 571-273-8300.

Most facsimile-transmitted patent application related correspondence is required to be sent to the Central FAX Number.

CENTRALIZED DELIVERY POLICY: For patent related correspondence, hand carry deliveries must be made to the Customer Service Window (now located at the Randolph Building, 401 Dulany Street, Alexandria, VA 22314), and facsimile transmissions must be sent to the Central FAX number, unless an exception applies. For example, if the examiner has rejected claims in a regular U.S. patent application, and the reply to the examiner's Office action is desired to be transmitted by facsimile rather than mailed, the reply must be sent to the Central FAX Number.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PHILIP J. SOBUTKA
PATENT EXAMINER

Philip J Sobutka

(571) 272-7887